Signal Flow Graph Modeling of Double-Gate RF MOSFET

Viranjay M. Srivastava, *Member, IAENG*

***Abstract* — For an electronic switch generally analysis is around analog and digitals systems. These are designed by the basic MOSEFT. The Double-Gate (DG) MOSFET is a renowned as the prime candidate for the scaling of MOSFET to the shortest channel length. To design the RF switch DG MOSFET can be used. Here a signal flow graph model of double-gate MOSFET has been analyzed, which can be used particularly for the Double-Pole Four-Throw (DP4T) switch in application of the wireless telecommunication systems. The signal flow graph of double-gate MOSFET operating at the frequency of microwave range has been investigated. From this double-gate MOSFET, RF switch can be designed, which will be capable to select the data streams from antennas for both the transmitting and receiving processes. In this paper the emphasis is on the basics of the circuit elements such as transfer function, switching characteristics required for the integrated circuit of the radio frequency sub-system of the double-gate CMOS switch.**

***Index Terms* — Control system, Double-gate MOSFET, RF switch, Signal flow graph, Transfer function, VLSI.**

I. Introduction

The CMOS switch uses the technique of Silicon on Insulator (SOI), which is attractive because of the high speed performance, low power consumption, scalability and effective potential [1]. The CMOS is suitable to integrate RF with digital circuits to design a system on a single chip. Due to these advantages, there has been growing interest in modeling of the RF CMOS. It is particular striking for various applications because it allows integration of both digital and analog functionality on the same die, with increasing performance at the same time as keeping system sizes reserved [2]. As compared to bulk silicon substrate, the architecture of SOI MOSFETs are more flexible due to several parameters such as thicknesses of film and buried oxide, substrate doping, and back gate bias which can be used for optimization and scaling [3-7]. It has various device structures such as Single-Gate (SG) MOSFET, Double-Gate (DG) MOSFET, FinFET, Cylindrical Surrounding (CS) MOSFET and Cylindrical Surrounding Double-Gate (CSDG, hollow cylinder structure) MOSFET. The DG MOSFET device structure with the help of signal flow graph modeling has been analyzed in this paper.

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Viranjay M. Srivastava is with the Department of Electronic Engineering, Howard College, University of KwaZulu-Natal, Durban - 4041, South Africa.

(Corresponding author phone: +27-31-260-2759; fax: +27-31-260-2740; e-mail: Viranjay@ieee.org, Srivastava@ukzn.ac.za).

Using the signal flow graph [8, 9], I had converted this DG MOSFET into a flow (block) diagram with the help of resistances and capacitances available in this MOSFET. After that the transfer function has been obtained, by which the equivalent circuit of this DG MOSFET has been analysed. This function can be used for further analysis of the device.

In this paper, I have presented a comprehensive study of signal flow graph of low power, high speed DG MOSFET, the effect of device geometry on working of this MOSFET and its switching properties. The organization of the paper is as follows. Double-gate MOSFET model with resistance and capacitance has been presented in the Section 2. Signal flow graph has been designed in the Section 3. Characteristics of the signal flow graphs have been discussed in the Section 4. Finally, the Section 5 concludes the work.

II. Resistive and Capacitive Model of Double-Gate MOSFET

In the communication system, to transmit or receive the information through the multiple antennas such as multiple-input multiple-output (MIMO) systems, it is essential to design a new RF switch that is capable of operating with multiple antennas and frequencies as well as minimizing signal distortion and power consumption [10]. Use of Silicon CMOS for these applications allows higher levels of integration and lower cost, also improving the efficiency [11]. Since DP4T switch is a fundamental switch for multiple-input, multiple-output data transfer applications because parallel data streams can be transmitted or received simultaneously using the multiple antennas and DG MOSFET is a unit cell to design this switch.

Fig. 1 presents a DG MOSFET, which has two gates G_1 (front gate) and G_2 (back-gate). The back channel has been probed by varying the substrate (back-gate) bias, with the front-gate voltage as a parameter [12]. Both gates control the channel from both side and provide additional gate length scaling by factor of two. The operation of ultra-thin transistors in double-gate mode brings significant advantages as scalability, ideal subthreshold slope, high current drive, and excellent transconductance.

A resistive and capacitive model of DG MOSFET, which is biased in linear region, at the ON state of switch is shown in Fig. 2. In this analysis the ON condition of the device has been taken into consideration, so that the maximum components of the device at their working condition and for

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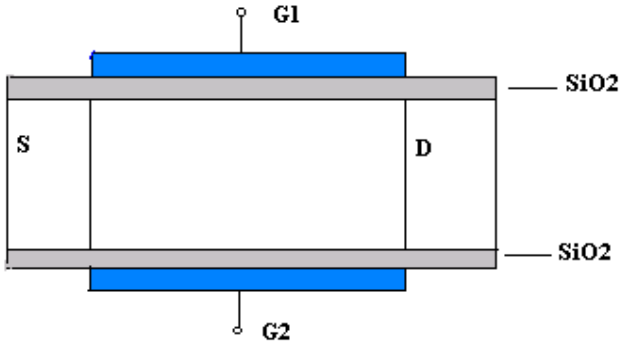

Fig. 1. Basic structure of the Double-Gate MOSFET.

obvious analysis of the device using worst condition. For the given design of double-gate MOSFET, under the operating condition, the insertion loss is conquered by its ON-resistance and substrate resistance [13].

The isolation of the switch is finite due to signal coupling through the parasitic and junction capacitances. Both the gates G_1 and G_2 control the channel in a good manner by selecting the channel width to be very small and by applying each gate contact to both sides of the channel. This process suppresses the short channel effects (SCE) and provides higher currents as compared with a traditional MOSFET. So both side's resistance and capacitance are used for the observation. The gate-1 components are with named as 1 and for gate-2 it is numbered as 2. At cut-off region, the MOSFET resistance R_{ON}, R_{ON1}, R_{ON2} will become zero. For maximum capacitance, assuming all the capacitances is active. In DG MOSFET, parasitic capacitances are C_{ds1}, C_{ds2}, C_{gs1}, C_{gs2}, C_{gd1} and C_{gd2}. These include the capacitance available due to the overlap between gate and source and between gate and drain. The junction capacitances are not present in the analysis as bulk is not available in this DG MOSFET. For DG MOSFET when both the transistors (upper and lower) are ON then C_{sb} and C_{db} are not present so fewer signals being coupled to the substrate as substrate is not present in this structure, so no dissipation in the substrate resistance R_b.

When the transistor is in cut-off region, increasing C_{ds1}, C_{ds2}, C_{gd1}, C_{gd2}, C_{gs1} and C_{gs2} leads to higher isolation between the source and drain, due to no capacitive coupling between these terminals. In the Fig. 2, for DG MOSFET, the total maximum capacitance across source to drain is:

$$C_{DG} = C_{ds1} + C_{ds2} + \frac{C_{gs1}.C_{gd1}}{C_{gs1} + C_{gd1}} + \frac{C_{gs2}.C_{gd2}}{C_{gs2} + C_{gd2}} \quad (1)$$

and the ON resistance will be combination of resistances due to gate 1 and gate 2 as follows:

$$R_{DG} = \frac{R_{ON1}.R_{ON2}}{R_{ON1} + R_{ON2}} \quad (2)$$

where

$$R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{gs} - V_{th})} \quad (3)$$

In general the p-type MOSFET switch has about three times the resistance of an n-type MOSFET switch of equal dimensions because electrons have about three times the mobility of holes in Silicon This resistive and capacitive model of DG MOSFET has been replaced by its impedance for signal flow model in following sections. For appropriate working of a switch and to reduce the insertion loss, we can also achieve reduction in ON-resistance with choosing transistor with large μ, increasing W/L, keeping V_{gs} - V_{th} large as clear from (3) [14].

III. Signal Flow Diagram of Equivalent Double-Gate MOSFET

The signal flow diagram has visualized input output relations, useful in design and realization of linear components. This helps to understand the flow of information between internal variables which are equivalent to a set of linear algebraic equations, mainly relevant where there is a cascade of information flow [15].

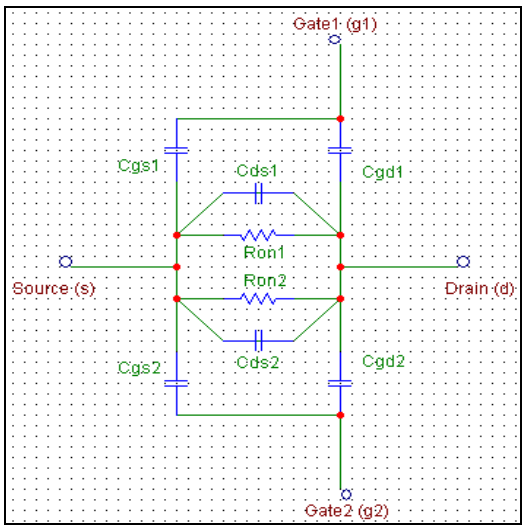

Fig. 2. Resistive and capacitive models of DG MOSFET operating as a switch at ON state.

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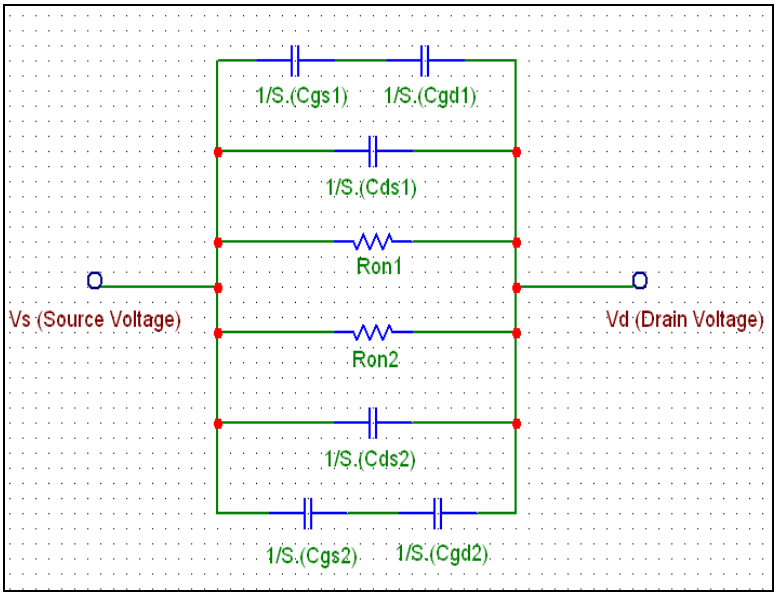

Fig. 3. Equivalent models of DG MOSFET with its Laplace transform.

In fig. 2, the source and the drain terminal are fixed and C_{gs1} is in series with C_{gd1} and C_{gs2} is in series with C_{gd2}. Now all these combinations are in parallel with C_{ds1}, C_{ds2}, R_{ON1}, and R_{ON2}. The current flow direction will remain same from drain to source and known as drain current I_{ds}. The block diagrams provide the details of configuration and interconnection of the components of an electronic system such as components available in the DG MOSFET. It can be used, together with transfer functions. With the help of model of DG MOSFET, I convert it into its equivalent Laplace Transform [16]. It is shown in Fig. 3, as all the capacitors are replaced by its impedances.

IV. Characteristics of Signal Flow Graph

The signal flow graph is a graphical representation of the flow of signals in the linear network which allows analysing its signals by simple visual inspection. To determine the characteristics of the DG MOSFET with the help of transfer function, the Laplace analysis on the Fig. 3 has been performed. The transfer function of a system is defined as the Laplace transform ratio of the output voltage to the input voltage [17, 18]. The equivalent impedance of the DG MOSFET as 'X' is shown in Fig. 4. It describes the flow of signals from one point of a system to another and provides the relationships between the signals, where x(t) and y(t) are the input signal and output signal respectively.

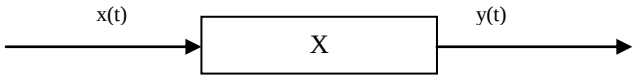

Fig. 4. Transfer function block model.

$$\frac{1}{X} = \frac{s.C_{gs_1}.C_{gd_1}}{C_{gs_1} + C_{gd_1}} + sC_{ds_1} + \frac{1}{R_{on_1}} + \frac{1}{R_{on_2}} + sC_{ds_2} + \frac{s.C_{gs_2}.C_{gd_2}}{C_{gs_2} + C_{gd_2}} \quad (4)$$

To calculate the transfer function following equation has been used:

$$V_d(s) = V_s(s) - I_{ds}.X(s) \quad (5)$$

where V_d and V_s are the drain voltage and the source voltage respectively and I_{ds} is drain to source current. So, the transfer function can be obtained as of the following format:

$$\frac{V_d(s)}{V_s(s)} = 1 - X(s)\frac{I_{ds}}{V_s(s)} \quad (6)$$

Here the Equation (6) shows the transfer function of the DG MOSFET extracted from the Fig. 3. By this transfer function one can conclude that this DG MOSFET can also be designed by a device whose transfer function is equivalent to the transfer function of Equation (6).

V. Result and Conclusions

In this paper, a symmetrical DG MOSFET has been modelled with signal flow graph in terms of its block diagram. After designing of the DG MOSFET, the schematic of the device at ON-state had been drawn. It includes the basics of the circuit elements parameter required for the radio frequency sub-systems of the integrated circuits such as resistance and capacitances available in the device. For the purpose of RF or microwave switch, I had achieved the process to minimize the components used to design the bulky MOSFET with help of the DG MOSFET. From the discussions in previous sections a single block model as in Fig. 4 had been obtained for the DG MOSFET model as shown in the Fig. 3. It means the MOSFET model using its transfer function can be verified.

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