Techniques of JFET Gate Capacitance Modeling

Stanislav Baná̌s, Josef Dobeš and Václav Paňko

***Abstract*—This paper presents various techniques and principles of modeling JFET gate capacitance. Various layout concepts as well as their gate capacitance measurements and modeling techniques are presented. Experience with potential modeling or measurement challenges is shared. The paper also deals with an often-omitted tight interaction between C-V and DC models, necessary for the well-fitting compact model. Good agreement has been achieved between measured silicon data and SPICE simulations for all discussed layout variants. Plots of various layouts and various tests from real production models are also presented.**

***Index Terms*—JFET, SPICE model, gate capacitance, pinch-off voltage, p-n junction barrier capacitance.**

I. Introduction

THE Junction Field Effect Transistor (JFET) is a component used in many applications, as for example low-noise amplifier, high input impedance amplifier, constant current source, etc. [1]. It can be constructed as 3-terminal (3T) or 4-terminal (4T) component. The more complicated 4T JFET contains two independently controlling gates, which allow two input signals to be applied simultaneously, so it can be used in signal mixing applications [2].

Development of JFETs especially for high-voltage applications requires considering various aspects, as for example optimization of breakdown voltage with series resistance, ESD robustness, etc. Therefore, various JFET concepts can be found. Apart from that, the JFET can be found as a parasitic structure in other components as for example in high-voltage PMOS, which can be observed in measured characteristics and should be considered in macro-model.

This paper is focused on the modeling of JFET gate capacitance, which is seemingly only a simple p-n junction, but in reality the measured C-V characteristics can at first look quite surprising. Various JFET concepts and measured gate capacitances including explained physical interpretation of observed phenomena are presented. Modeling techniques (lumped model, behavioral model, etc.) are compared and plots with silicon data vs simulated results are demonstrated.

II. Single-gate (three-terminal) JFET

The example of single-gate JFET cross-section is shown in Fig. 1, the related layout is in Fig. 2 and the typical macro-model is in Fig. 3. Such component is often called the pinch resistor and it is often used as a constant current source.

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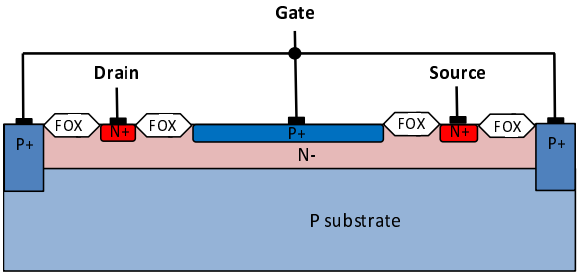

Fig. 1. Cross-section of single-gate JFET (pinch resistor).

Voltage dependent capacitances C_{GD} and C_{GS} are usually represented by the compact diode SPICE models with the voltage dependent p-n junction barrier capacitance described by the equation [3], [4]

$$C = \frac{C_{\mathrm{j0}}}{\left(1 - \frac{V}{V_{\mathrm{j}}}\right)^{M_{\mathrm{j}}}} \mathrm{AREA} \qquad (1)$$

where C_{j0} is the zero-bias junction capacitance per unit area, V_{j} is junction built-in potential, M_{j} is grading coefficient, and AREA is the area of pn junction (representing the half of JFET gate area).

These compact diode SPICE models can be either part of customized lumped macro-model or integrated in the JFET model as for example in R3 model [5].

It is apparent, that low doped substrate and high doped P+ gate are connected in our three-terminal JFET, so the question is, how to measure and evaluate model parameters of C_{GD} and C_{GS} for the equation 1. The equation assumes a physical p-n junction with depletion area spreading with the applied p-n junction voltage, not two parallel p-n junctions affecting each other.

One of possible solutions is to measure the gate and substrate p-n junctions separately and implement two parallel diodes in the model instead of one. However, such solution does not correctly represent the real situation, where the JFET channel can be pinched off by a few volts. The separate measurements in artificial structures do not cover this case.

It is more correct to measure the real situation of gate and substrate connected in a real JFET device. In such a case,

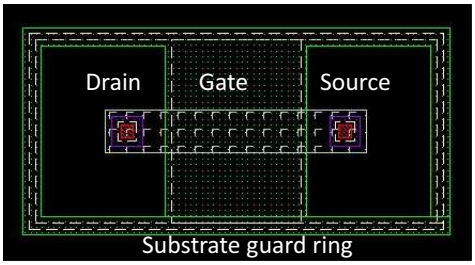

Fig. 2. Layout of single-gate JFET (pinch resistor).

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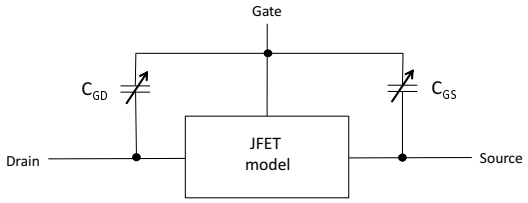

Fig. 3. Simplified C-V macro-model of single-gate JFET (pinch resistor).

however, the extracted parameters V_j and M_j can get quite far from their expected physical values, which especially occurs at low temperatures. In compact models the parameter V_j has the integrated temperature dependency [3]

$$V_J(T) = V_J(T_\mathrm{nom})\left(\frac{T}{T_\mathrm{nom}}\right) + 2V_t ln\left(\frac{n_i(T_\mathrm{nom})}{n_i(T)}\right) \quad (2)$$

where T is simulation temperature, T_nom is nominal reference temperature at which the values of basic model parameters were extracted, V_t is the thermal voltage and n_i is the intrinsic carrier concentration of used material, in our case silicon, with its own temperature dependency [3]

$$n_i(T) = n_i(T_\mathrm{nom})\left(\frac{T}{T_\mathrm{nom}}\right)^{X_{ti}} \exp\left(\frac{q}{2k}\left(\frac{\mathrm{E_G(T_{nom})}}{T_\mathrm{nom}} - \frac{\mathrm{E_G(T)}}{T}\right)\right) \quad (3)$$

where X_{ti} is intrinsic carrier concentration temperature exponent used in SPICE as a tunable temperature parameter, typically set to the value 1.5, and E_G is the gap width with its own temperature dependency described in [6].

Therefore, if the extracted V_J value gets too far from its expected physical value, it can become too low at very low temperatures, and making V/V_j too dominant, in extreme case even larger than 1, which could cause negative capacitance. The extracted parameters should thus be carefully verified in the full temperature range. If the verification fails and obtaining precise voltage dependent capacitance with the integrated model equation 1 becomes impossible, the alternative solution of behavioral voltage dependent capacitor model can be used.

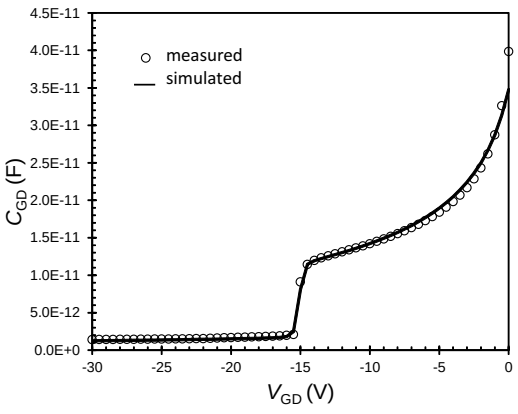

Fig. 4. C_{GD}-V characteristic of single-gate JFET with full depletion at $V_\mathrm{GD} = -15$ V.

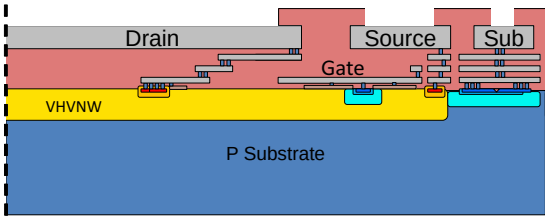

Fig. 5. Cross-section of high-voltage dual-gate 4T JFET.

In any case it is necessary to measure the gate capacitance in the real three-terminal structures containing drain, source and gate terminals, and not (as is often practised) in large two-terminal customized p-n junction structures. If the JFET is too small and gate capacitance value is under tester measurement limit (sometimes called measurement noise floor), more JFETs in parallel can be used instead. Correct measurement of gate-drain capacitance C_{GD} is with floating source, correct measurement of gate-source capacitance C_{GS} is with floating drain.

Let us for simplicity only talk about measurement of gate-drain capacitance C_{GD} in the following text. In such a case the measured gate-drain capacitance C_{GD} is equal to the sum of two parallel capacitances: gate-drain capacitance (direct p-n junction) and gate-source capacitance in series with the source-drain resistance, which is basically a JFET represented by its DC model. When the gate-drain voltage V_{GD} voltage across the p-n junction reaches the JFET pinch-off voltage, the JFET body becomes fully depleted, and the mentioned second parallel path containing gate-source capacitance C_{GS} is disconnected. This appears as a steep drop of capacitance in measured C-V characteristic, as demonstrated in Fig. 4. Measurement of the gate capacitance with shorted drain and source does not show this effect. The same effect was observed also in gate capacitances of MESFET/pHEMT or microwave varactors [7].

III. Dual-Gate (Four-Terminal) JFET

An example of dual-gate JFET cross-section is shown in Fig. 5, the related layout is in Fig. 6 and the typical macro-model is in Fig. 7. This component is designed for high-voltage applications, therefore it has a circular or oval shape with the high voltage pad in the center, as illustrated in Fig. 6. This configuration ensures that the high voltage applied to

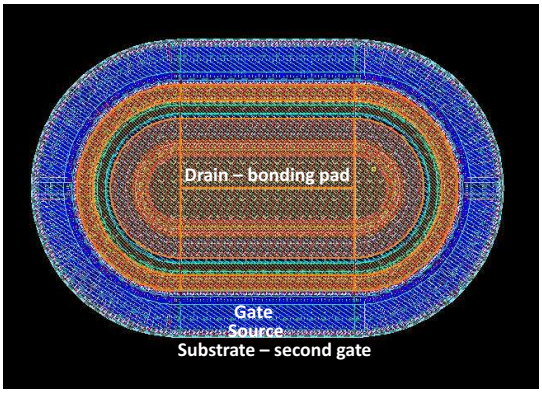

Fig. 6. Layout of high-voltage dual-gate 4T JFET.

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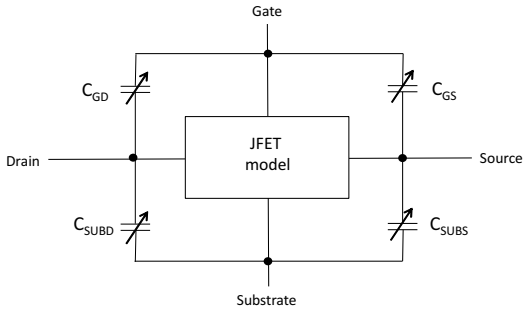

Fig. 7. Simplified C-V macro-model of dual-gate 4T JFET.

the drain appears only in vertical direction in the center of the oval where the high breakdown voltage is ensured by low concentration of carriers in the substrate. Sufficient drift length or other techniques (e.g. double RESURF [8]) make sure that this high voltage does not appear in the device's perimeter and the device can operate at such high voltages [9]. Examples of the dual-gate JFET applications can be found in [10].

In the case of dual-gate JFET there are two effective gates (gate and substrate) represented by two p-n junctions, so there are four voltage dependent capacitors in the macro-model, as depicted in Fig. 7. Therefore, four C-V tests must be measured: Gate-drain capacitance C_{GD} with floating source, substrate-drain capacitance C_{SUBD} with floating source, gate-source capacitance C_{GS} with floating drain and substrate-source capacitance C_{SUBS} with floating drain. The principle is analogous with that described in previous section for single gate JFET, but in this case the measurement of gate capacitances has substrate voltage as a parameter and the measurement of substrate capacitances has gate voltage as a parameter.

The measured characteristics as well as the simulated curves are presented in Fig. 8 and Fig. 9. Fig. 8 shows gate-drain capacitance C_{GD} measured for various substrate voltages. It is apparent, that the substrate voltage is affecting the pinch-off voltage V_{GD}, because the pinch-off voltage of dual-gate JFET is affected by depletion areas of both gates. The more dominant gate is the one with higher concentration of carriers, because the diffusion of minor carriers to the JFET body is higher in this case. This can be demonstrated

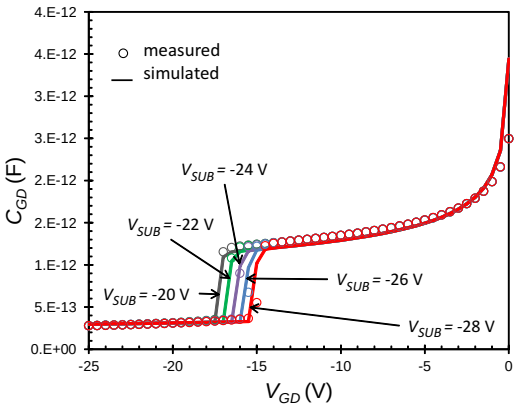

Fig. 8. C_{GD}-V characteristic of high-voltage dual-gate JFET with parametrized V_{SUB} = -20, -22, -24, -26, -28 V.

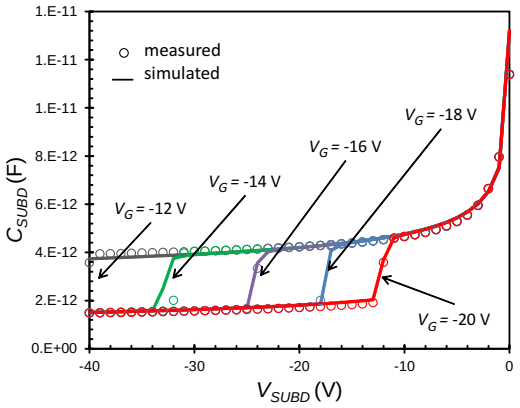

Fig. 9. C_{SUBD}-V characteristic of high-voltage dual-gate JFET with parametrized V_G = -12, -14, -16, -18, -20 V.

by the comparison of Fig. 8 and Fig. 9, where the same step of second parameter has different impacts: the gate charge is apparently more concentrated and therefore the gate voltage V_G in Fig. 9 has a higher impact on the pinch-off voltage than the substrate voltage V_{SUB} does in Fig. 8.

As mentioned in previous section, a well-fitting DC model (especially for pinch-off voltage) is a necessity for the correct precise low-signal capacitance model. For the dual-gate JFET it is even more challenging, because the pinch-off voltage is determined by a combination of both gate voltages V_G and V_{SUB} and each of them has a different impact. Various behavioral DC models of dual-gate JFET are published for example in [2] or in [9].

The next challenge for the dual-gate JFET gate capacitance modeling is the device with a non-uniform JFET channel. Fig. 5 shows a JFET with gate covering only a smaller part of JFET channel. In such a case the gate-drain capacitance is in reality a p-n junction capacitance in series with a very-high-voltage Nwell (VHVNW) layer not covered by the gate. Ideal modeling solution would be the macro-model of dual-gate JFET in series with single gate JFET and the gate-drain capacitance would rather be the capacitance between gate and internal node between the two mentioned JFETs. Such a solution directly corresponds with the layout, but it is overly complicated, difficult for the parameter extraction (how can these two segments be measured separately?) and predisposed to convergence issues.

Another possible modeling solution is using the standard barrier capacitance of equation 1, but unfortunately with a high probability of the extracted parameters far from their physical values and thus the temperature model failing, as explained in section A. So the verification in full temperature

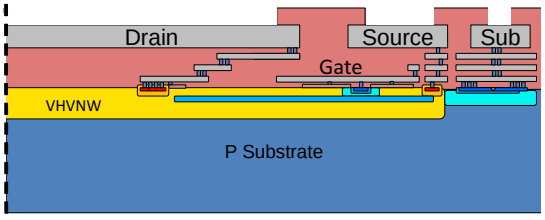

Fig. 10. Cross-section of high-voltage dual-gate 4T JFET with parasitic surfact channel.

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range is again necessary.

The last proposed modeling solution is using the customized behavioral voltage dependent capacitance. It is preferred to model the capacitance with a charge controlled model as recommended in [11].

IV. Dual-gate (four-terminal) JFET with parasitic surface channel

A high-voltage JFET does not necessarily have to have non-uniform channel. Fig. 10 demonstrates JFET described in previous section, in this case with the additional buried-layer gate covering almost whole the JFET channel. However, this construction has another challenge, consisting in the parasitic JFET channel between silicon surface and buried gate.

In such case the gate-drain capacitance is predominantly located in the parasitic JFET channel between the surface and buried layer, while the majority of current flows via the main channel under buried layer. Measurement of such gate-drain capacitance with substrate voltage as a parameter and floating source is shown in Fig. 11. Unlike in the previous tests, in this case the gate was grounded while the drain voltage being swept on. Therefore, $-V_{DG}$ instead of V_{GD} is on X-axis. This information is important only for correct understanding of parameter V_{SUB}. Measured is the gate-drain capacitance C_{GD} like in previous tests.

At low gate-drain voltages the measured capacitance is composed of the surface gate-drain capacitance, the main channel gate-drain capacitance and the gate-source capacitance in series with JFET. At about $V_{GD} = 15V$ the parasitic surface channel becomes depleted and the surface gate-drain capacitance becomes disconnected. Because it was the dominant one, the measured capacitance significantly drops down. In the range of gate-drain voltage between about 15V and 20V the main channel gate-drain capacitance and the gate-source capacitance in series with JFET are significant. And finally at $V_{GD} > 20V$ the main JFET channel gets fully pinched, with the pinch-off voltage affected by the applied substrate voltage, as detailed Fig. 12. This effect was explained in previous section. In other words, the substrate voltage affects only the second capacitance drop at $V_{GD} > 20V$, while the rest of the C-V curve is substrate-voltage independent.

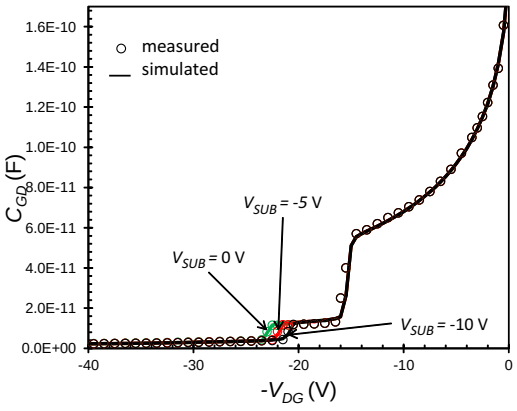

Fig. 11. C_{GD}-V characteristic of high-voltage dual-gate JFET with parasitic surface channel and parametrized V_{SUB} = 0, -5, -10 V affecting the pinching of main JFET channel.

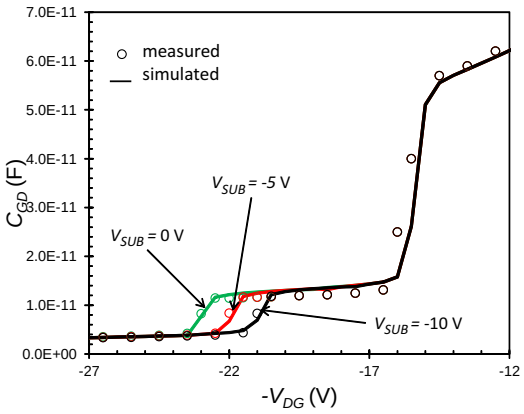

Fig. 12. C_{GD}-V characteristic of high-voltage dual-gate JFET with parasitic surface channel and parametrized V_{SUB} = 0, -5, -10 V, focused to disconnection of "source path" due to pinched main JFET channel.

The modeling of the second capacitance drop is covered naturally by the combination of precise DC model of dual-gate JFET [2], [9] and four related voltage dependent capacitances (compact diode SPICE models). The modeling of the first dominant capacitance drop can be done by two possible methods.

The first one was demonstrated in [9]. The gate-drain surface channel capacitor is modeled by a behavioral voltage-dependent capacitor using equation 1 multiplied with the multiplication factor C_{mult}

$$C_{\mathrm{mult}} = \left(\sqrt{(V_{\mathrm{GD}} + V_{\mathrm{poff}})^2 + V_{\mathrm{st}}} + 0.5 - \sqrt{(V_{\mathrm{GD}} + V_{\mathrm{poff}} - 0.5)^2 + V_{\mathrm{st}}} \right) \quad (4)$$

where $V_{\mathrm{GD}} = -V_{\mathrm{DG}}$ is the gate-to-drain voltage, V_{poff} is the gate capacitance pinch-off voltage and V_{st} controls the steepness of the gate capacitance drop.

The approximate behavior of (4) is

for $V_{\mathrm{GD}} \leq -V_{\mathrm{poff}}$:	$C_{\mathrm{mult}} = 0$
for $V_{\mathrm{GD}} \in (-V_{\mathrm{poff}}, -V_{\mathrm{poff}} + 0.5)$:	$C_{\mathrm{mult}} \in (0, 1)$
for $V_{\mathrm{GD}} \geq -V_{\mathrm{poff}} + 0.5$:	$C_{\mathrm{mult}} = 1.$

The voltage-dependent gate-drain capacitance is then defined as

$$C_{\mathrm{GD}} = C_{\mathrm{mult}} \frac{C_{\mathrm{j0}}}{\left(1 - \frac{V_{\mathrm{GD}}}{V_{\mathrm{j}}}\right)^{M_{\mathrm{j}}}} AREA \quad (5)$$

This solution, however, brings a risk of convergence errors in transient analysis, as mentioned in [11], where the charge-controlled model is recommended. Another possible solution is to implement the surface parasitic JFET channel in the macro-model as a JFET DC model and put it in series with the substrate gate-drain capacitor. The disadvantage of this is the increase of model complexity. However, it is close to the natural layout, which is usually a good solution.

V. Parasitic JFET in other components

As mentioned earlier, the JFET device, especially for high side applications, can be constructed in different ways which should be taken into account during model development. Previous sections demonstrated only some examples of possible JFET types.

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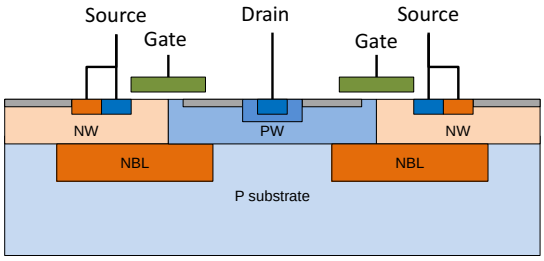

Fig. 13. Cross-section of high-voltage PMOS with parasitic drain JFET (p-type). N-body shorted to P-source represents JFET gate (n-type).

In Fig. 13 the cross-section of another component, in this case high voltage PMOS, is shown, where the drain-source capacitance is affected by the parasitic JFET created by the P-substrate channel and two N buried layers (NBL) representing JFET gate. This PMOS has its bulk shorted with the source, so the measured output drain-source capacitance for negative V_{DS} might be expected to be the simple barrier capacitance with voltage dependency described by the equation 1. But the data shows a similar capacitance drop as in Fig. 4, which is caused by the pinching of the mentioned parasitic JFET. In this case the drain-source capacitance must be modeled, similarly as the surface parasitic channel described in previous section, either by behavioral voltage dependent capacitance or by the implementation of parasitic JFET in the lumped macro-model.

Similar parasitic JFETs can appear also in other component types, as for example bipolar transistors, diodes, etc. So a careful measurement using the right measurement setup and considering this phenomena in the final model are necessary to obtain an accurate model representing the real electrical behavior of the device.

VI. Conclusion

JFET gate capacitance is often considered to be just a simple p-n junction. Its measurement and careful modeling is therefore often underestimated. This capacitance is however usually affected by the pinching JFET effect, which must be taken into account. It was demonstrated, that JFET can appear also as a parasitic component in other electrical components and must be also considered in the macro-model. Various examples were presented and for each of them various techniques and principles of modeling gate capacitance were proposed. Some plots with measured silicon data and simulated models were demonstrated.

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